1. General Description

QS6400 is a high quality sound DSP for mobile phones that plays music through a built-in ADPCM decoder with sound font rom.
QS6400 is equipped with HWASS's QPCM synthesizer,which is capable of generating up to 64 voices with different tones.
QS6400 can also play two channels of wavefiles of differing sampling rates.
Since data in the FIFO buffer is processed on demand, the length of the data(MIDI & WAVE) is not limited, making QS6400 an excellent platform for applications such as incoming melody distribution service.
The MIDI handler built in to QS6400 can play MIDI data without an extra buffer.
Included is a PWM module for audio out with a maximum output of 500mw at 8Ω load registance(PVDD=4.0V).
For earphone use, QS6400 provides a single-ended stereophonic output terminal.
To operate QS6400 to full capability, "Standard MIDI File(SMF) Format 0" is recommended.

2. Features

➢ADPCM synthesizer functions
- 64 voices generated at 39kH simultaneously.
- Compatible with stereophonic sound generation.
- Master Volume control
  Individual channel volume / master volume.
- Built-in MIDI handler(sequencer)
- Equipped with two buffers of 128 bytes FIFO for MIDI play.
- Built-in 4 bit or 8 bit ADPCM decorder.

➢TONE
- Supports GENERAL MIDI LITE specification.
  GM 128 voices + 47 voices percussion.
  Support to control parameters by "BxH xxh"(see the MIDI implementation chart)
- Additional 8 voices to play korean traditional music.
  Gayagum/Daegum/Haegum/Taepyoungso/Buk/Ggwengary/Jang-goo/Jing.
- Various sampling rate : 8 ~ 39Khz

➢ WAVE
- Support to playback ADPCM wavefile(2 Channels)
- Separate wave volume control(0~255).
  Gayagum/Daegum/Haegum/Taepyoungso/Buk/Ggwengary/Jang-goo/Jing.

➢ CPU INTERFACING
- 14 Wires parallel interfacing

➢AUDIO OUTPUT

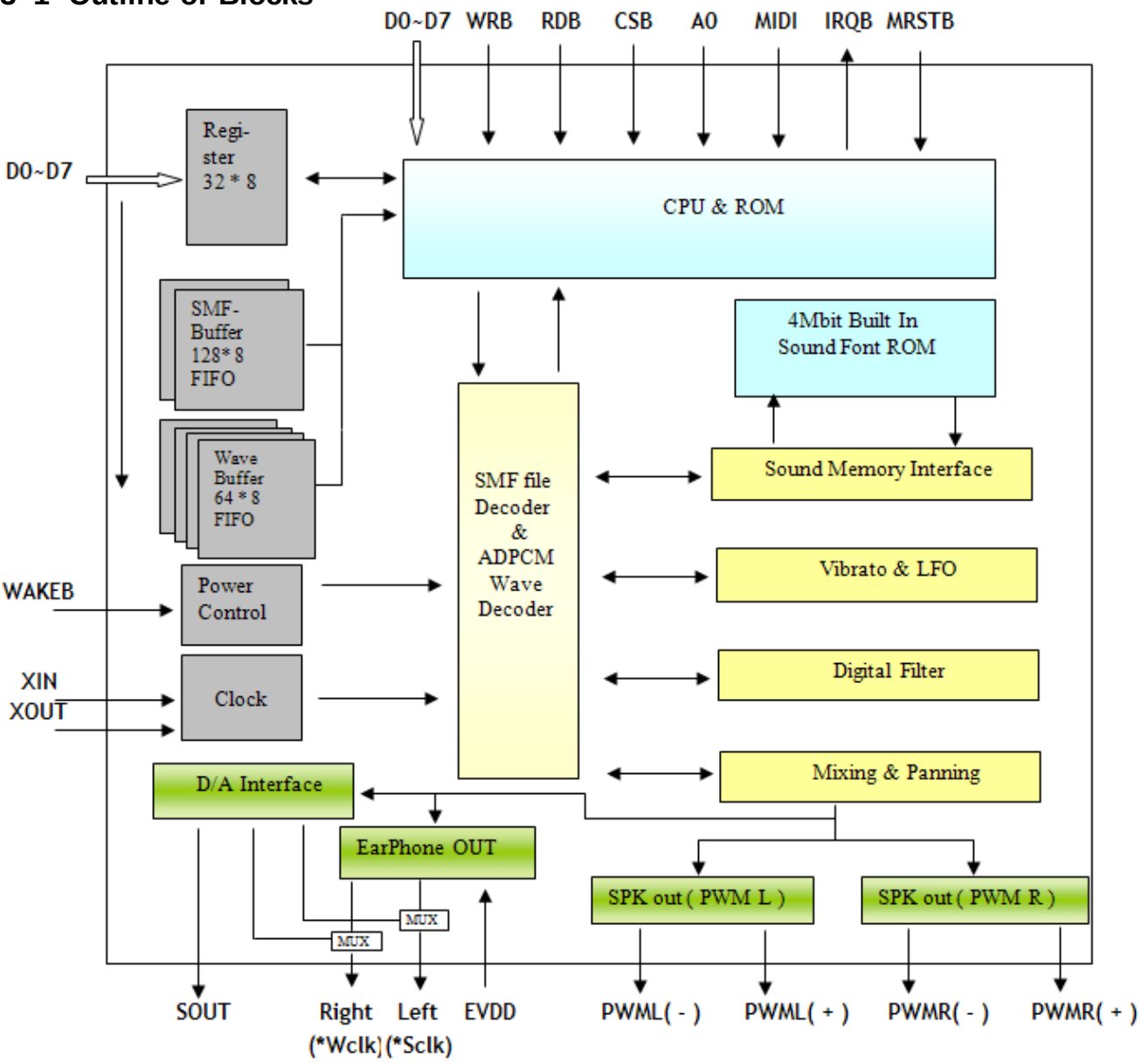
- PWM or 16bit DAC output can be selected.
- PWM output mode : 500mW when PVDD=4.0V, RL=8Ω
- Provides Stereo or Mono output for earphone.

➢POWER SUPPLY

- Includes three power supplies for sub-system
  PVDD power supply devoted to PWM block.(3.3 ~ 4.2V)
  EVDD power supply devoted to earphone block.(2.7 ~ 3.6V)
  VDD is normal power supply.(2.7 ~ 3.6V)

3. Block Diagram

3- 1 Outline of Blocks



3- 2 Description of Blocks

Explanations about each block of QS6400 and flows of the signal are as follows.

1) Register Block : QS6400 has registers of 32 x 8 for storing control data.
Built-in 8052 can communicate directly with the register blocks, which are used to change control values and communicate commands. 23 x 8 registers are used for this purpose.
The extra registers are available to support additional features.

2) SMF FIFO buffer : This FIFO is used in receiving SMF file blocks (128bytes) from Host. SMF FIFO Buffer has two banks of memory block and each buffer is filled with data according to REG_IREQ_TYPE (When bit 2 is "1") from built- in 8052. When receiving a data request (IRQB) for the next procedure you should read the interrupt request type register (REG_IREQ_TYPE) to check which data is required.

3) WAVE FIFO buffer : This FIFO is used in receiving wave data blocks (64 or 128 bytes) from Host. WAVE FIFO Buffer has four banks of memory block, of 64 bytes each. The buffer size is determined by user specification (using REG_WAVE_CHAN). Each bank is filled with wave data accoding to REG_IREQ_TYPE(when bit 1 or bit 0 is "1") If you intend to play high-sampling-rate(up to 22khz) wave files, we recommend that you use only one wave channel, due to the high transmission rate of data. In this case, WAVE FIFO Buffer size is preset to 128bytes.

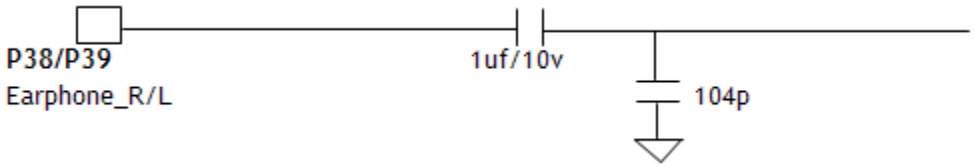
4) Power control : This block is in charge of power management.
You can select whether to enter or wake-up from power down mode.

5) Clock generator : This block is a clock generator for the internal master clock.
QS6400 need the external clock input to operate normally.

6) CPU & ROM : This block describes 8052 micom and 12k bytes program ROM memory.
Built-in 8052 interprets SMF and Wave file.

7) PWM Speaker out : This block converts audio data into PWM format.
It supports stereophonic audio out.
You can also mute this output.

8) Earphone out : This block converts audio data into single-ended earphone signal.
You should connect poled-capacitor and bypass capacitor.



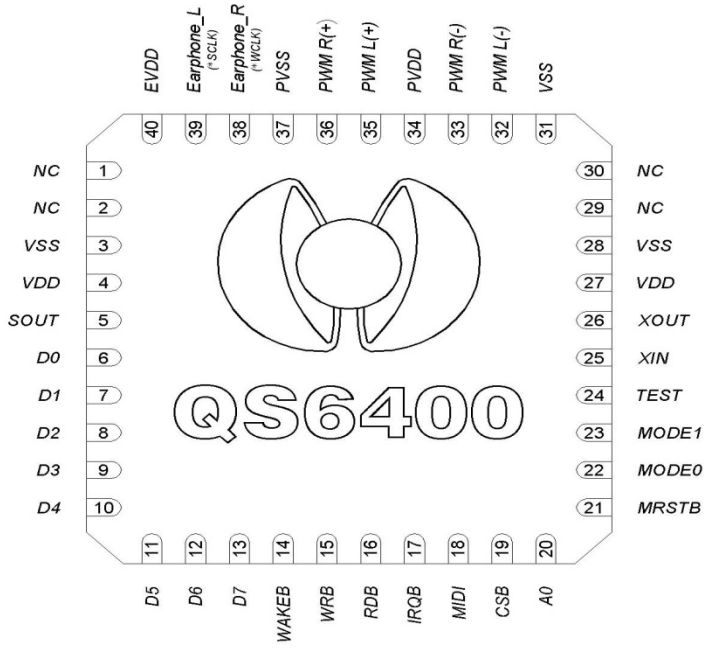
9) D/A interface : This block generates 16bit DAC interfacing out for high quality sound. If you have an additonal DAC, you can also use this interfacing out. When you use the DAC OUT mode, earphone is disabled.

10) Sound font : This is an embedded maskrom for GM 128 sound map and 47 percussion. The sound font built in this device stores the sampling data according to GM 128 sound map. Additionally QS6400 has sampling data to support korean traditional music.

4. Pin Rotation and Descriptions

4- 1 Pin Rotation

4-1-1 40P MLF



4- 2 Pin Rotation

PIN NO	PIN NO	PIN NAME	I/O	DESCRIPTION
-	1	NC	X	No Connect
1	2	NC	X	No Connect
2	3	NC	X	No Connect
3	4	VSS	P	Ground
4	5	VDD	P	Power Supply
5	6	SOUT	O	Serial Data Out for DAC
6	7	D0	I/O	Bidirection DATA BUS
7	8	D1	I/O	Bidirection DATA BUS
8	9	D2	I/O	Bidirection DATA BUS
9	10	D3	I/O	Bidirection DATA BUS
10	11	D4	I/O	Bidirection DATA BUS
-	12	NC	X	No Connect
-	13	NC	X	No Connect
11	14	D5	I/O	Bidirection DATA BUS
12	15	D6	I/O	Bidirection DATA BUS
13	16	D7	I/O	Bidirection DATA BUS
14	17	WAKEB	I	WakeUp Signal(Active Low)
15	18	WRB	I	Write Enable
16	19	RDB	I	Read Enable
17	20	IRQB	O	Request Data Block(Active Low)
18	21	MIDI	I	MIDI IN (UART)
19	22	CSB	I	Chip Select
20	23	A0	I	Register Address or Data Strobe
-	24	NC	X	No Connect
-	25	NC	X	No Connect
21	26	MRSTB	I	Master Reset (Active Low)
22	27	MODE0	I/O	LED control port or test mode
23	28	MODE1	I/O	Vibrator control port or test mode
24	29	TEST	I	Test Mode Select(must be Low)
25	30	XIN	I	Master Clock In
26	31	XOUT	I	MODE0 and MODE1 I/O select
27	32	VDD	P	Power Supply
28	33	VSS	P	Ground
29	34	NC	X	No Connect
30	35	NC	X	No Connect
-	36	NC	X	No Connect
-	37	NC	X	No Connect
31	38	VSS	P	Ground
32	39	PWML(-)	O	PWM Output Left (-)
33	40	PWMR(-)	O	PWM Output Right (-)
34	41	PVDD	I	PWM Power
35	42	PWML(+)	O	PWM Output Left (+)
36	43	PWMR(+)	O	PWM Output Right (+)
37	44	PVSS	I	PWM Ground
38	45	EarPhone_R(*Wclk)	O	EarPhone out Right or Word Clock for DAC
39	46	EarPhone_L(*Sclk)	O	EarPhone out Left or Serial Clock for DAC
40	47	EVDD	P	Power for EarPhone

4- 3 Detail pin descriptions.

➢POWER SUPPLY PINS

- VDD (4,27)
- These pins are connected to a normal power supply.
- VSS (3,28,31)
- These pins are GNDs of power.
- PVDD(34), EVDD(40),PVSS (37)
- PVDD is VDD for PWM block. It's capable of driving a voltage of MAX 4.2V down to 3.3V.
- EVDD is VDD for EarPhone block. Its range covers 3.6V to 2.7V.
- PVSS is PWM block GND.

➢POWER RESET

- MRSTB (21)
- Reset is accomplished by holding the MRSTB pin low for at least 60 oscillator periods while the oscillator is running. To ensure proper power-on reset, the MRSTB pin must be high long enough to allow the oscillator time to start up plus 40 oscillator periods.
- RESET should be free from glitch noise.
- At power-on, the voltage on VDD and MRSTB must come up at the same time for a proper start-up.
- After RESET, all registers and internal RAM are initialized to "0x00“

➢ AUDIO INTERFACE

- Support to playback ADPCM wavefile(2 Channels)
- Separate wave volume control(0~255).
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➢ CPU INTERFACING

- 14 Wires parallel interfacing